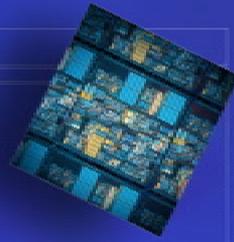


February 25th, 2004

廣田 洋一

マーケティングマネージャ
インタープライズ & ネットワークソリューションズ 本部
インテル株式会社



Empowering new frontiers in HPC

Intel HPC Technologies

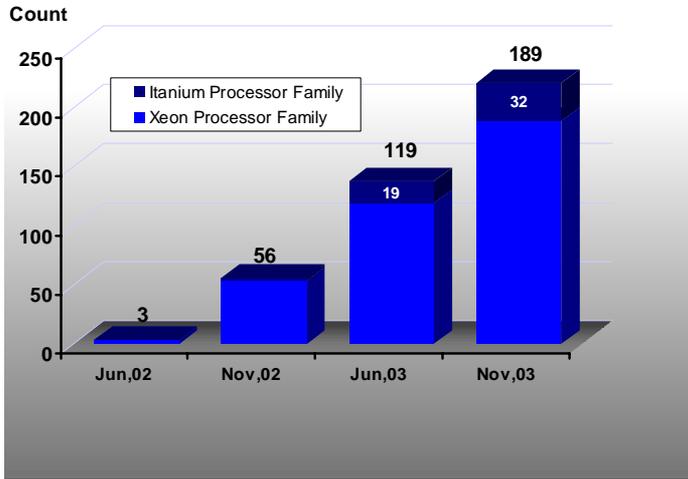
Intel® and Top 500

- 189 Intel-based systems on Top500 list
 - MSS leader with 37% of system being iA based, displacing RISC architectures
 - November 2002: 56 systems to November 2003: 189 systems
 - >40% of deployments into commercial segments
- 40% of top ten systems
 - NCSA (#4), Lawrence Livermore Nat'l Lab (#7, #10), Pacific Northwest National Labs (#5)
- Intel® Itanium® processor-based systems
 - From 19 systems in June to 32 in November

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2

Intel and Top500

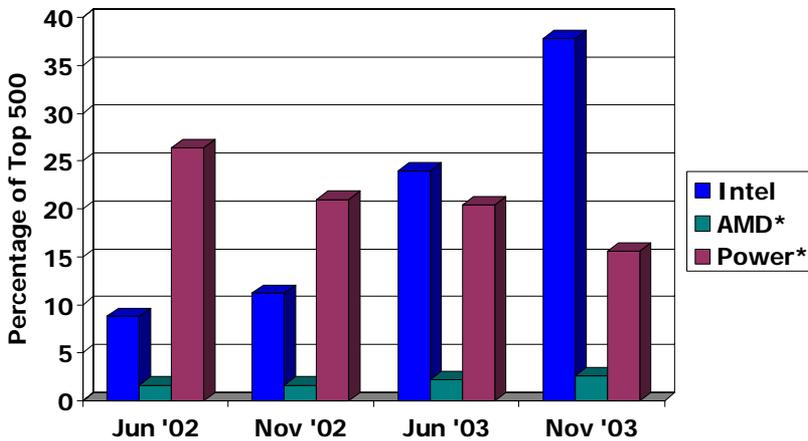


Source: Latest TOP500 list, Nov. 2003. Data available at: www.top500.org/lists



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Intel® and Top 500

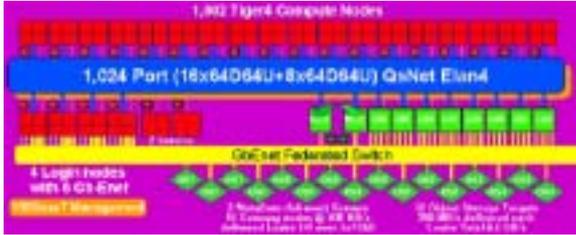


Source: www.top500.org



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New Proof Point: Thunder



- From Concept to Deployment in Five Months
- Target Performance of 20TFLOP Peak
- Highest Performance COTS based solution in the world
- Approximately 3,840 Intel® Itanium® Processors



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Intel® Itanium® 2 Processors Today



Available SKUs for DP and MP:
 1.5 GHz, 6MB iL3 Cache
 1.4 GHz, 4MB iL3 Cache
 1.3 GHz, 3MB iL3 Cache



1.4 GHz, 1.5MB iL3 Compute Optimized DP
 1.0 GHz, 1.5MB iL3 Cache Low-Voltage DP



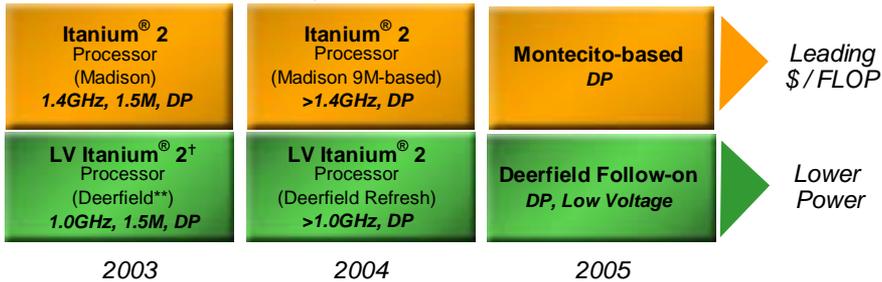
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Intel® Itanium® 2 Processor Family

Multi-Processor (MP) Capable



Dual Processor (DP) Capable



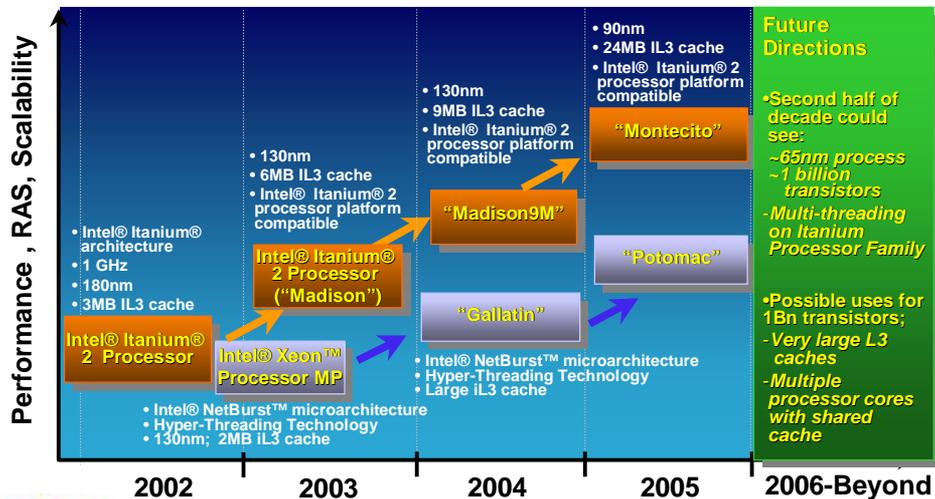
† Low Voltage Intel® Itanium® 2 processor

All products, dates and information are preliminary and subject to change without notice



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Intel® Architecture MP Server Processor Roadmap



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Montecito** Summary

- Intel's first dual core processor
- Intel's first processor with > 1 billion transistors
- 24MB L3 Cache
- Multithreading
- 90 nanometer process technology
- Socket compatible with previous Itanium 2-based systems
- Target 2005 platform release



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Moore's Law

~1.1x Moore's Law

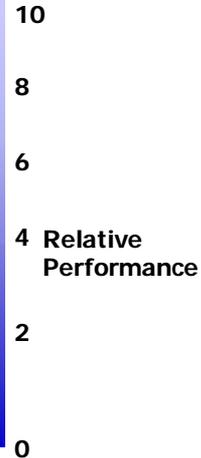


+10% to +20%

>2x Moore's Law

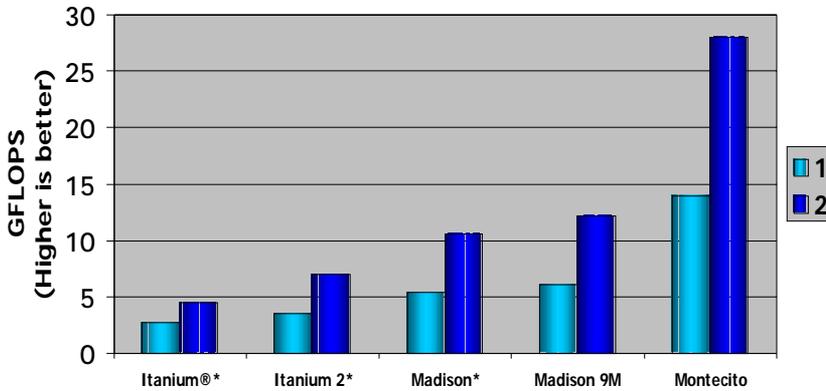


+30% to +50%



**Q2 '03* is a performance range based on an average increase measured and estimated across workloads that include: SPECint2000, SPECpb2000, SPECweb99_SSL, TPC-C, and SAP SD 2-tier benchmarks on 4-way servers with Intel Itanium® processor at 1.5 GHz with 6MB L3 cache and Intel Xeon™ MP processor at 2.8 GHz with 2MB L3 cache.
* 3 Year performance is based on Intel Interconnects and Intel I/O and Chipsets.
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Linpack Projections



*Actual data

Processors

All projections based on Intel estimates. Note: Madison 9M and Montecito roughly use Itanium 2 processor efficiency and scaling values, with some extrapolation for bandwidths

Performance tests and ratings are measured using specific computer systems and/or components and reflect the approximate performance of Intel products as measured by those tests. Any difference in system hardware or software design or configuration may affect actual performance. Buyers should consult other sources of information to evaluate the performance of systems or components they are considering purchasing. For more information on performance tests and on the performance of Intel products, reference www.intel.com/performance or call (U.S.) 1-800-628-8686 or 1-916-356-3104



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Intel Silicon Technologies

A new process every 2 years

Process Name	P856	P858	Px60	P1262	P1264	P1266	P1268
1 st Production	1997	1999	2001	2003	2005	2007	2009
Lithography	.25µm	.18µm	.13µm	90nm	65nm	45nm	32nm
Gate Length	.20µm	.13µm	<70nm	<50nm	<35nm	<25nm	<18nm
Wafer Size (mm)	200	200	200/300	300	300	300	300

Production

Development

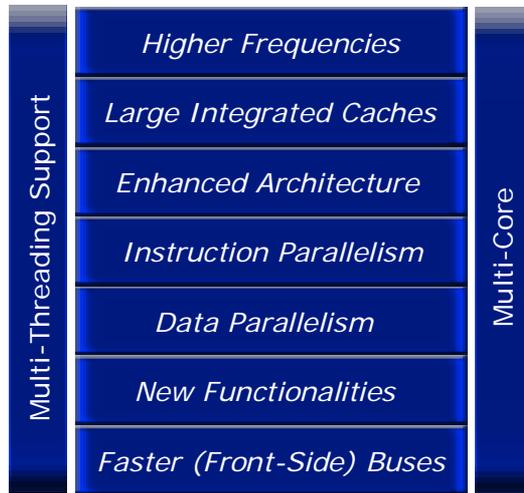
Research

All dates specified are target dates provided for planning purposes only and are subject to change.



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Processor Architecture Directions



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Summary

The Economics of High-Performance Computing have changed.

High-Performance Computing solutions must track Moore's law to be viable.

Intel is playing a key role in accelerating HPC solutions for science, engineering and business with open commercial off the shelf technology leadership.